Synch. Buck Regulated by a digital PWM

The schematic "SyncBuck_Digital_PWM.sxsch" in this example directory contains the schematic of a synchronously rectified buck converter regulated by a digital controller. The digital controller is made up of hierarchical child components and the user is encouraged to descend down the hierarchy to see the internal details of the example digital controller. This example digital controller is provided as an example on how the SIMPLIS advanced digital components can be put together to model a digitally controlled voltage regulator.

This digital controller has the following features:

1) A master clock of 1 GHz.
2) The ON-time resolution of the PWM1 output is simply set to the period of the master clock, which would be 1 ns.
3) The switching period T_{SW} is set to 2048 ns, which yields a switching frequency f_{SW} of approximately 488.28 kHz.
4) The feedback voltage at the VFB1 pin is sampled once per switching period. Thus, the sampling frequency f_S is same as the switching frequency f_{SW}. Better performance could have been achieved with a higher sampling rate. For the sake of simplicity, this example digital controller is set to have one sampling per switching period and the sampling is taken at almost the end of each switching cycle, before the MOSFET is commanded to turn on.
5) The analog feedback voltage is converted to a digital quantity by a 9-bit A-to-D converter. The 9-bit output space of the A-to-D converter is set up to cover the range of 0 to 2.5 V of the input space.
6) To control the ON-time output, a compensator implemented with digital adders, subtractors, multipliers, and registers and various logic gates is employed.

The power stage has the following parameters:

1) A pair of complex poles at f_{LC} = 4.886 kHz due to the energy-storage inductor and the output capacitors.
2) A zero due to the ESR of the output capacitors at $f_{Z,ESR}$ =37.15 kHz.
3) A voltage divider with a transfer ratio of H_{FB} = 0.5.
4) An input voltage of range of 4.5 to 5.5 V.

The digital compensator needs to be designed according to the parameters of the power-stage to yield stable and robust voltage regulation.

The loop gain $T(s)$ of the regulated converter is

$$T(s) = H_{FB}\, G_{ADC}\, G_{COMP}(s)\, G_{PWM}\, G_{PS}(s) \tag{1}$$

G_{ADC} is the gain of the A-to-D converter (ADC), ignoring any high-frequency sampling effect. It is the ratio of the digital output to the analog input error. If we define the resolution of the ADC as Q_{ADC} then the gain of the ADC is

$$G_{ADC} = 1/Q_{ADC} \tag{2}$$

In our case, $Q_{ADC} = 2.5/2^9 = 4.883\times10^{-3}$ V.

$G_{COMP}(s)$ is the transfer function of the digital compensator to be designed.

G_{PWM} is the gain of the PWM. It is defined as the gain from its input to the produced duty ratio. If the input to the digital PWM is a multiple-bit integer and an increase in the LSB of this integer would lead to an increase in resolution of τ_{PWM} in the ON-time, then

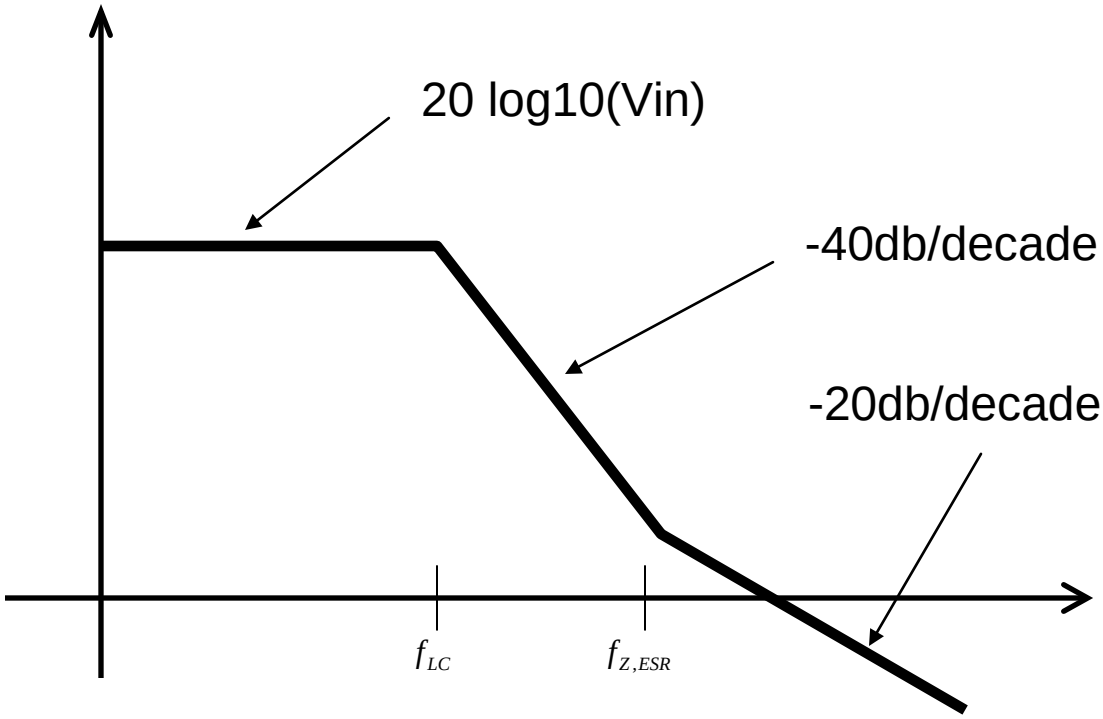
$$G_{PWM} = \tau_{PWM}/T_{SW} \tag{3}$$

In our case, $G_{PWM} = 1\times10^{-9}/2048\times10^{-9} = 1/2048 = 4.883\times10^{-4}$.

$G_{PS}(s)$ is the transfer function of the power stage. It is the transfer function from the duty ratio produced by the digital controller to the output voltage. Its DC gain is equal to the input voltage, and it has a pair of complex poles at f_{LC} caused by the output filter and a zero at $f_{Z,ESR}$ due to the ESR of the output capacitor(s).

$$G_{PS}(s) = \frac{V_{IN}(1+s/s_{Z,ESR})}{1+(2\varsigma\, s/s_{LC})+(s^2/s_{LC}{}^2)} \tag{4}$$

ς is the damping ratio. The following diagram shows a simplified plot of the magnitude of $G_{PS}(f)$ versus frequency. To simplify, the complex poles were plotted as if they were a pair of real poles at the same frequency.



The goal is to design the compensator so that the overall loop gain $T(s)$ has as large a bandwidth as possible and as high a DC gain as possible and yet maintain stability. This can be achieved if the magnitude of the overall loop gain $T(s)$ has a slope that is approximately −20dB/decade across the spectrum from DC to the frequencies around cross-over. This will ensure that the phase margin will be close to 45 degrees or higher.

To achieve this goal, the compensator needs to have a pole at $f_{P1} = 0$, two zeros at f_{Z1} and f_{Z2} at frequencies lower than f_{LC} to counter the effect of the pair of complex poles, and a pole at f_{P2} at a frequency twice as high as $f_{Z,ESR}$ so as to allow the zero at $f_{Z,ESR}$ to provide some phase boost to the loop gain but yet not significantly changing the slope of the magnitude of the loop gain. Thus, $G_{COMP}(s)$ can be expressed as:

$$G_{COMP}(s) = \frac{A\,(1 - s/s_{Z1})(1 - s/s_{Z2})}{s\,(1 - s/s_{P2})} \tag{5}$$

In this example, $G_{COMP}(s)$ is designed to have the following parameters:

$$\begin{aligned} A &= 64.88 \times 10^3 \\ s_{Z1} &= -9000 + j5756 \\ s_{Z2} &= -9000 - j5756 \\ s_{P2} &= -306.8 \times 10^3 \end{aligned} \tag{6}$$

The pole associated with s_{P2} is located at about 48.828 kHz, which is higher than $f_{Z,ESR}$ and it is still at or below one-tenth of the sampling frequency. The two zeros associated with s_{Z1} and s_{Z2} are complex, with a damping ratio of 0.84 and an undamped natural frequency of 1.7 kHz. The choice of the complex zeroes is somewhat arbitrary here. A pair of real zeros could have been located in the frequency range of 1 kHz to 3 kHz.

While the compensator transfer function $G_{COMP}(s)$ can be synthesized in the discrete domain in canonical form, the digital controller in this example employs a discrete PID compensator to achieve this transfer function. This allows those users who are familiar with PID compensators to change the PID coefficients to see how the regulated system responses varies according to the changes in the PID coefficients.

The following analog PID transfer function is used to achieve the transfer function $G_{COMP}(s)$ shown in (5):

$$T_{PID}(s) = K_{PA} + \frac{K_{IA}}{s} + \frac{K_{DA}s}{\gamma K_{DA}s + 1} \tag{7}$$

A pole has been added to the differential term so that $T_{PID}(s)$ has two poles and two zeros. Matching (7) against (5), and with the constants defined in (6) substituted in, we have

$$\begin{aligned} \gamma K_{DA} &= (-1/s_{P2}) = 3.259\times10^{-6} \\ K_{IA} &= A = 64.88\times10^{3} \\ K_{PA} &= -A\left[(1/s_{Z1}) + (1/s_{Z2})\right] - K_{IA}\,\gamma K_{DA} = 10.02 \\ K_{DA} &= A/(s_{Z1}s_{Z2}) - K_{PA}\,\gamma K_{DA} = 535.8\times10^{-6} \\ \gamma &= 3.259\times10^{-6}/K_{DA} = 6.08210^{-3} \end{aligned} \tag{8}$$

Using the bilinear transformation, which is also known as the trapezoidal-rule for integration and differentiation, the transfer function (7) in the s-domain is mapped to the discrete z-domain by replacing s with $\frac{2(z-1)}{T_S(z+1)}$ where T_S is the sampling period. Thus,

$$T_{PID}(z) = K_{PA} + \frac{K_{IA}T_S}{S(z)} + \frac{(K_{DA}/T_S)S(z)}{\gamma(K_{DA}/T_S)S(z) + 1} \tag{9}$$

where

$$S(z) = \frac{2(z-1)}{z+1} \tag{10}$$

The transfer function in (9) can be rewritten as:

$$
\begin{aligned}
T_{PID}(z) &= K_P + \frac{K_I}{S(z)} + \frac{K_D S(z)}{\gamma K_D S(z) + 1} \\
K_P &= K_{PA} = 10.02 \\
K_I &= K_{IA} T_S = 132.8 \times 10^{-3} \\
K_D &= K_{DA} / T_S = 261.6
\end{aligned}
\tag{11}
$$

For ease of debugging and inspecting the output of the proportional, integral, and differential terms, the discrete PID compensator in this example digital controller is implemented in the parallel form instead of the canonical form.

The proportional term is a straightforward scaling by the constant K_P and does not need any further elaboration here.

The integral term represents:

$$
\frac{O_I(z)}{I_I(z)} = \frac{K_I}{S(z)} = \frac{K_I(z+1)}{2(z-1)} = \frac{(K_I/2)(1+z^{-1})}{(1-z^{-1})} \tag{12}
$$

The difference equation representing this discrete transfer function is:

$$
O_I(n) = O_I(n-1) + (K_I/2)\big(I_I(n) + I_I(n-1)\big) \tag{13}
$$

The difference equation (13) is implemented in the I_term component inside the PID_compensator component.

The differential term represents:

$$
\frac{O_O(z)}{I_O(z)} = \frac{K_D S(z)}{\gamma K_D S(z) + 1} = \frac{2K_D(z-1)}{(2\gamma K_D + 1)z + (1 - 2\gamma K_D)} \tag{14}
$$

Substituting the values of γ and K_D into the denominator of (14) yields

$$
\begin{aligned}
\frac{O_O(z)}{I_O(z)} &= \frac{2K_D(z-1)}{(2\gamma K_D + 1)z + (1 - 2\gamma K_D)} \\
&\approx \frac{2K_D(z-1)}{4.182\, z - 2.182} \\
&= \frac{K_D(z-1)}{2.091\, z - 1.091} \\
&\approx \frac{K_D(z-1)}{2\, z - 1} \\
&= \frac{K_D(1-z^{-1})}{2 - z^{-1}}
\end{aligned}
\tag{15}
$$

The difference equation representing this discrete transfer function is:

$$O_O(n) = \left[O_O(n-1) + K_D\left(I_O(n) + I_O(n-1)\right)\right]/2 \tag{16}$$

The difference equation (16) is implemented through the D_term and the D_term_low_pass components.

Obviously, K_P, K_I, and K_D have to be stored either as constants or parameters in the example digital controller. With the example digital controller using integer arithmetic instead of fixed-point arithmetic, these three coefficients need to be scaled large enough to be stored as integers with sufficient significant bits. Hence, in the PID_coefficents component, $16K_P$, $2048K_I$, and $16K_D$, instead of K_P, K_I, and K_D, are stored.

The A-to-D converter employed in a digital controller will convert analog signals into integers or fixed-point quantities, thus introducing quantization of the signals. The DPWM in a digital controller can only command pulsewidths in discrete time resolution, thus introducing the effect of discretization of time. The POP and AC analyses in SIMPLIS work with infinitesimally small quantities and, thus, cannot be applied to analyze a system where there is quantization of the signals or the discretization of the timing signals that are used to control the power stage. To help the user to inspect the ideal small-signal AC loop gain of this example digital controller, an analog equivalent of the digital controller has been provided here for convenience.

The schematic "A_SyncBuck_Digital_PWM_POP_AC_Transient.sxsch" in this example directory contains the same power stage as the one shown in the schematic "SyncBuck_Digital_PWM.sxsch" but the controller involved is an analog equivalent of the digital controller. This analog-equivalent controller has the following features:

1) The switching period T_{SW} is set to the same 2048 ns as the digital controller.

2) The feedback voltage at the VFB1 pin is not sampled. The 9-bit A-to-D converter is replaced by a linear gain of $2^9/2.5$.

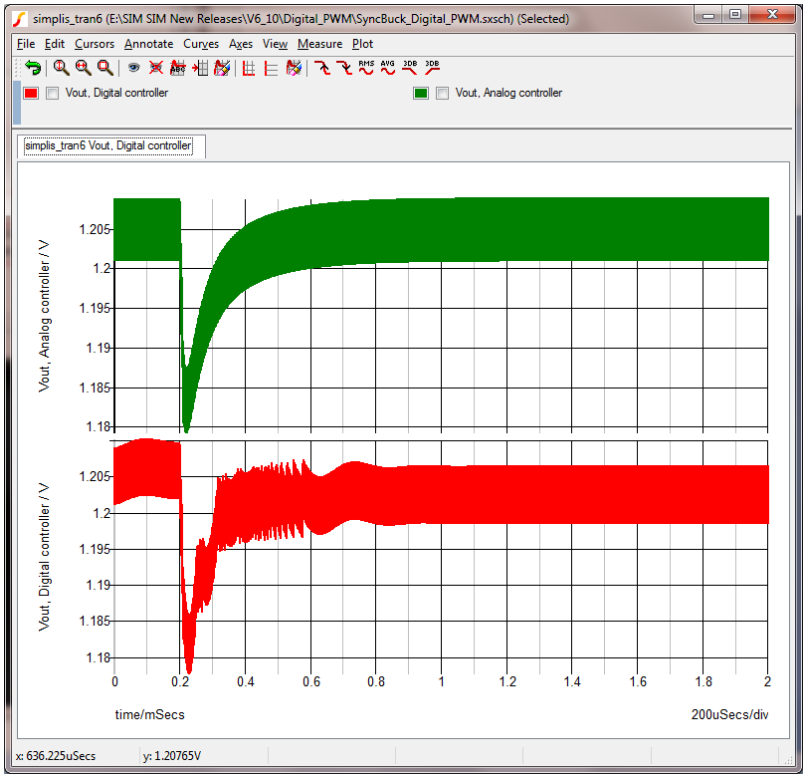
3) The PID compensator is implemented with a discrete-time PID filter. This filter will sample its input signal but it will not quantize its outputs. The sampling frequency of this discrete-time PID filter is set to the same sampling frequency of the digital controller and the PID coefficients have been set to the same values as those used in the digital PID compensator.

4) To control the ON-time output, an analog PWM is employed so that it can adjust the ON-time in a continuous manner instead of in discretized increments. It has been designed so that for every one unit increase in its input, the output duty ratio will increase by 1/2048, same as the PWM in the digital controller. The only difference is that, in the analog-equivalent controller, the input to the PWM are not restricted to integers.

5) The signal levels inside the analog version of the controller have been set to match those in the digital controller, even though some of the signal levels may be unrealistic for an analog controller. For example, the A_Vref component is set to provide a 123 V reference since its digital counterpart is providing the decimal integer 123 as its output.

The schematic "A_SyncBuck_Digital_PWM_POP_AC_Transient.sxsch" has been set up to first run the POP analysis to figure out the periodic operating trajectories of this closed-loop regulated converter, then run the AC analysis to figure out the loop gain, and then run a subsequent load transient analysis

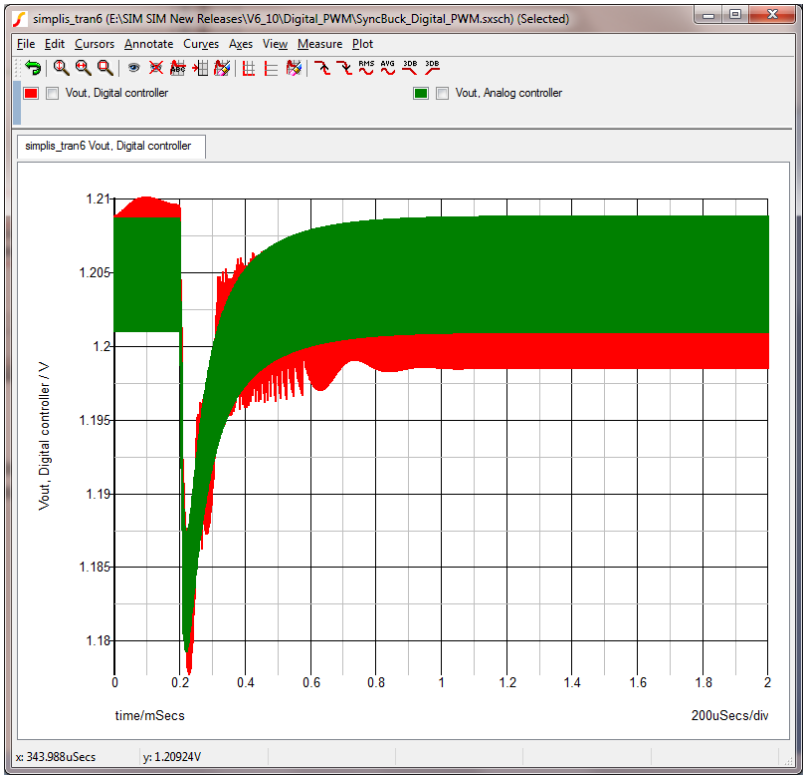
The following plot shows the comparison of the output voltage of the two schematics under the same load transient condition.



The bottom waveform shows the output voltage of the schematic with the digital controller and the top waveform shows the output voltage of the schematic employing the analog-equivalent controller. The two waveforms are very close to each other.

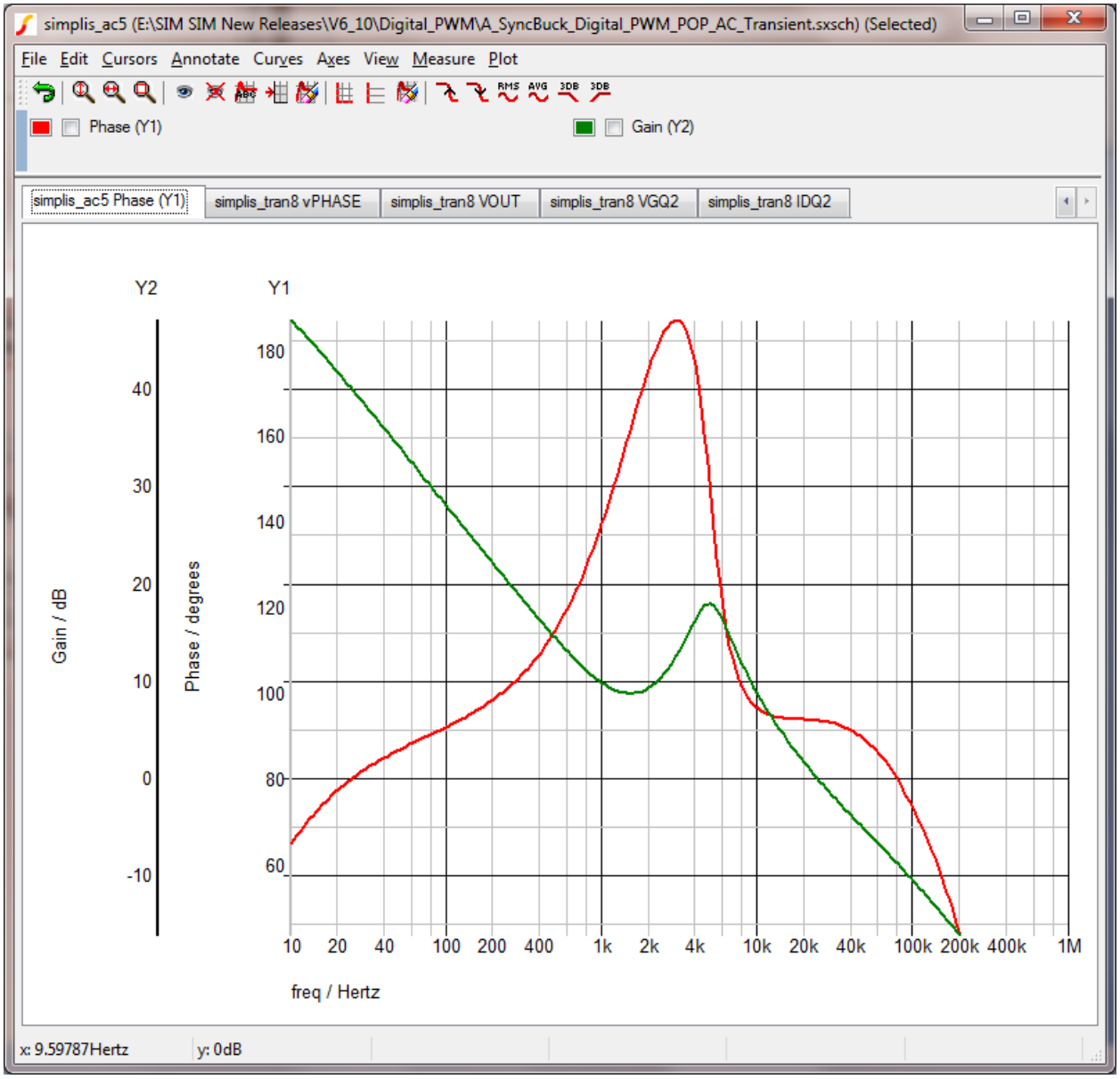
The output voltage of the converter with the digital controller shows some high-frequency jittery during the transient recovery. This is caused by the quantization of the A-to-D and the discretization of the ON-time in the digital controller. For the analog-equivalent controller, these two effects are not present and the controller can continuously adjust the ON time once every switching cycle.

The following is the re-plotting of the same two waveforms, but with them stacked on top of each other with the same y-axis.



Other than the high-frequency jittery, the two waveforms match quite well during the transient recovery part. As the two converters recover towards the new steady states, the output voltage of the converter regulated by the digital controller is slightly lower than the output voltage of the analog version. This slight difference is due to the fact that the feedback voltage at the VFB1 pin is already within one bin size of the A-to-D converter from the reference value. Thus, as far as the A-to-D converter is concerned, this feedback voltage matches the reference value. Hence, the error component produces a zero output, and the input to the PID compensator is zero, and there will be no further adjustment to the ON-time. The output voltage will stay at the value according to the discretized ON-time and the losses in the power stage. Once the feedback voltage stays long enough within one bin size of the A-to-D from the reference value, the net effect is an open-loop operation where the ON-time is fixed, and the remaining small changes in the output voltage resembles the typical 2nd-order response of the power stage when it is not under close-loop control. This is evident from the output voltage of the digital version starting at about 0.6 ms in the plot.

The Bode plot of the loop gain of the converter regulated by the analog-equivalent controller is provided here for reference.


simplis_ac5 (E:\SIM SIM New Releases\V6_10\Digital_PWM\A_SyncBuck_Digital_PWM_POP_AC_Transient.sxsch) (Selected)
File Edit Cursors Annotate Curves Axes View Measure Plot
Phase (Y1)
Gain (Y2)
simplis_ac5 Phase (Y1)
simplis_tran8 vPHASE
simplis_tran8 VOUT
simplis_tran8 VGQ2
simplis_tran8 IDQ2
Y2
Y1
Gain / dB
Phase / degrees
freq / Hertz
x: 9.59787Hertz
y: 0dB