



## New Advanced Digital Simulation with SIMPLIS v5.6

### Major Benefits

To support and enhance the simulation of switching power supplies containing large amounts of digital content, we have introduced the new SIMPLIS Advanced Digital simulation capability. SIMPLIS v5.6 :

- Makes **Virtual prototyping** of mixed mode analog and digital circuits in power conversion applications practical regardless of the level of digital content.
- Provides in the **Advanced Digital Library** a wide variety of new digital functions to simplify your simulation efforts.
- **Improves simulation speed by 10-20x** for basic digital gate simulation compared to earlier versions of SIMPLIS.

SIMPLIS 5.6 allows designers of digitally controlled power supplies to effectively explore the interaction between increasingly complex digital control schemes and the resulting performance of the complete power supply system. SIMPLIS 5.6 also improves the simulation speed of power supply systems with significant digital content describing supervisory and protection circuits.

### New Digital Features

The **Advanced Digital Library** provides a wide variety of new digital functions to simplify your simulation efforts.

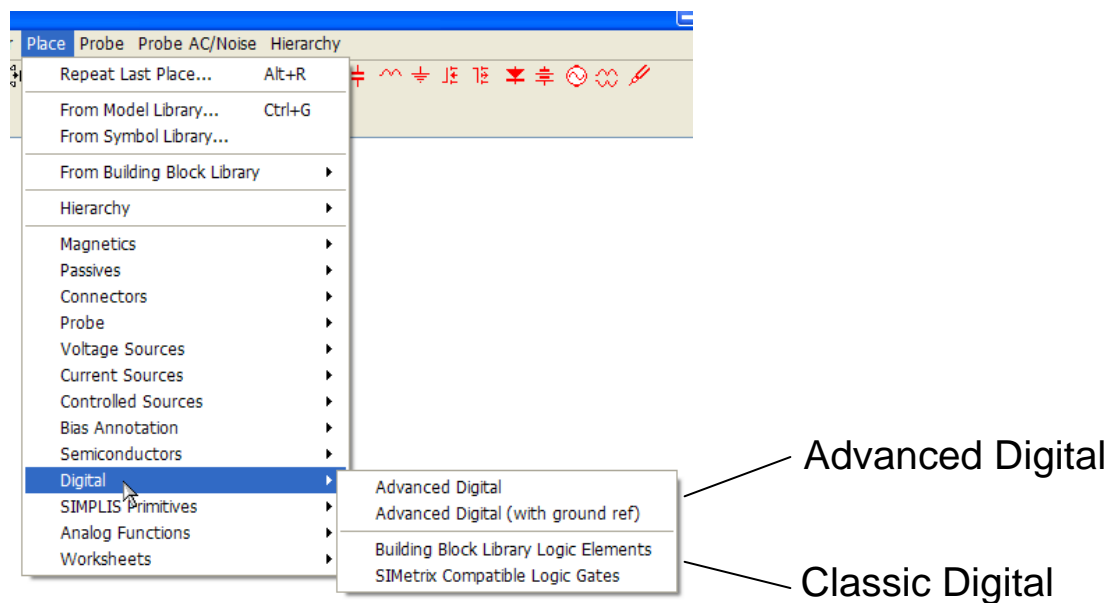
- In addition to the basic logic gates that have long been included in the SIMPLIS engine, the library now includes:
  - Adders
  - Subtracters
  - Multipliers
  - Comparators
  - Counters
  - ADCs
  - Expanded library of flip-flops and latches
  - Asymmetric Delay Block
- All new logic functions in the Advanced Digital library have improved characteristics including :
  - Inertial delay on inputs. (Input glitches narrower than the specified delay are effectively ignored rather than being propagated through the device.)
  - Finite delay in all Advanced Digital devices. (This eliminates problems associated with the classic SIMPLIS logic gate's ability to instantaneously switch state with zero delay.)

- Random bus probe feature is now available for use on any digital bus containing all Advanced Digital nodes at any level of a hierarchical schematic
- Ground Reference pin is optional when connected to all Advanced Digital devices

## Advanced Digital Components

SIMPLIS v5.6 enhances the digital simulation performance of the traditional SIMPLIS simulation engine. This enhanced digital simulation capability specifically works with the simulation of the new Advanced Digital components. The improved simulation speed of Advanced Digital components in SIMPLIS v5.6 results in a much faster and more efficient overall simulations when there is a significant amount of digital content in the system under study.

We refer to the new digital components as “Advanced Digital components” while referring to the traditional digital models in SIMPLIS as the “classic digital components.” Beginning with SIMPLIS v5.6, both classic and Advanced Digital components are supported and they are both available for placement on the schematic through a reorganized set of menus in the schematic editor.



All Advanced Digital components have four slanted stripes in the lower left-hand corner of the symbol. For example, a 3-input AND gate will look like one of the following, where U1 has a ground-reference pin and U2 does not:



## Classic Components

A component is considered a classic component if it meets all of the following requirements:

- 1) It is NOT an Advanced Digital component.
- 2) It is NOT a probe that measures voltage. For example, the regular voltage probe, the bus voltage probe, and the Bode plot probe are all probes that measure voltages.
- 3) It is NOT a fixed pin current probe.

Hence, resistors, capacitors, inductors, independent and controlled sources, transformers, BJTs, MOSFETs, opto-couplers, fixed in-line current probes, etc. are all considered classic components. A classic digital component is also considered a classic component as its simulation performance is unchanged by the new enhanced digital simulator.

## Similarities between Classic and Advanced Digital Components

- 1) Both classic digital components and Advanced Digital components employ similar analog parameters for modeling the input behavior. Typically, each input pin is modeled by an analog-to-digital interface bridge composed of a resistor  $R_{IN}$ . Each input pin is modeled by a logic state of 0 or 1, depending on the value of the input voltage as compared to the threshold voltage  $TH$  and the hysteretic-window width  $HYSTWD$ .
- 2) Both classic and Advanced Digital components employ similar analog parameters for modeling the output behavior. Typically, each output is modeled by a digital-to-analog interface bridge that is composed of a resistor  $R_{OUT}$  in series with a voltage source. The voltage source will have a value of  $V_{OL}$  or  $V_{OH}$ , depending on the logic output state of that output pin.
- 3) Both classic and Advanced Digital components support devices with or without the ground reference pins, with a few minor exceptions.
- 4) Both classic and Advanced Digital components model the switching of the outputs with zero rise time and zero fall time.

## Differences between Classic and Advanced Digital Components

- 1) While Advanced Digital components support analog parameters for modeling the input or output behavior, an A-to-D or D-to-A interface bridge is introduced if and only if the particular input or output pin is connected to a classic component. If an input or output pin of an Advanced Digital component is connected only to other Advanced Digital components, the probing of such a node will produce a waveform of logic values of 0, 1, or 0.5 (for an indeterminate logic value) versus time and it will be plotted as digital data in the upper portion of the waveform display tool. If you try to random probe the pin *current* of such a pin, the result will be a constant current of zero amperes since there is no analog circuitry to model the input or output behavior of such a pin. That is, if an input or output pin of an Advanced Digital component is connected only to other

Advanced Digital components, the input associated with such an input or output pin exists only in the logical space and not in the analog space.

- 2) For an Advanced Digital component, the ground reference pin **MUST** exist if at least one of the input pins or one of the output pins is connected to a classic component.

When all of the input pins and all of the output pins of an Advanced Digital component are connected only to other Advanced Digital components, the ground reference pin is optional. Its presence or absence will not impact the simulation results.

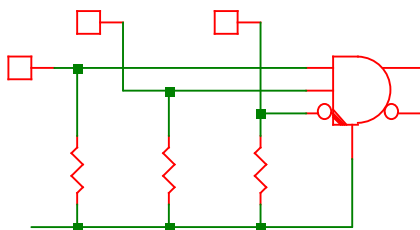
- 3) For a classic digital component without ground reference pin, each output produces an analog voltage through its Thevenin equivalent output with respect to the ground node in the schematic.
- 4) While the delay parameter is optional and has a default value of 0.0 in the classic digital components, the *delay parameters* in the Advanced Digital components are mandatory and they *are not allowed to be equal to 0.0*.
- 5) The classic digital components employ the “transport” delay model, which means for simple logic gates any glitches in the inputs are passed along to the output(s) after the defined delay. The Advanced Digital components employ the “inertial” delay model and *glitches in the inputs that are shorter than the output-delay parameter are absorbed by the digital component and are not passed along to the output(s)*.

## Strategies for Deploying the new Advanced Digital Components

The key to an efficient simulation using new SIMPLIS Advanced Digital components is to achieve the optimum balance between taking maximum advantage of the faster simulation times for Advanced Digital components while minimizing unnecessary interaction between new Advanced Digital components and the rest of the classic components in the SIMPLIS schematic. This can be accomplished using the following guidelines:

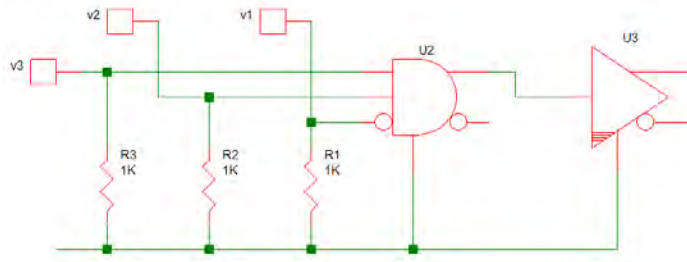
- 1) Isolate Advanced Digital components as much as possible and try to locally minimize the number of I/O pins that are connected to classic components.
- 2) If most or all inputs to a simple logic gate are required to be connected to classic components, the simulation will run faster if a classic digital component is used as a front-end to drive a buffer from the Advanced Digital component library.

For example, if all inputs to a three-input AND-gate are connected to classic analog components, a valid option is to have an Advanced Digital 3-input AND gate to sense the three analog inputs directly:



However, for a more efficient and faster simulation, you should re-arrange the circuit and use a classic 3-input AND gate from the building-block library as the front-end to drive an Advanced Digital buffer. This approach is faster because the classic simulation engine

only interrupts the Advanced Digital simulation when the logic state of the output of U2 changes, whereas, in the former case the classic simulation engine has to interrupt the Advanced Digital simulation any time one of the three inputs of the AND-gate changes logic state.



In this example, you should assign zero delay to U2, the classic 3-input AND gate and the non-zero delay to U3, the Advanced Digital buffer.

- 3) For an Advanced Digital component that has at least one I/O pin connected to an analog node, *you must use the version that includes the ground reference pin.*
- 4) For an Advanced Digital component whose I/O pins are all connected only to other Advanced Digital components, either the version that includes the ground reference pin or the version that does not include the reference pin can be used. The choice is up to the preference of the user and will not impact the simulation results.

## A Simple DEMO Circuit

At our website you may download a hierarchical schematic representing a simple synchronous buck converter controlled by a PWM controller employing PID compensation.

[http://simplistech.com/downloads/resources/example\\_circuits](http://simplistech.com/downloads/resources/example_circuits)

This PWM controller is entirely made up from new Advanced Digital components.

## Limitations in this v5.6 release

- 1) SIMPLIS v5.6 has the same POP and AC analysis capability as the current SIMPLIS v5.5. So in v5.6, if you take an existing 5.5 SIMPLIS schematic that runs POP and AC analysis and then substitute an Advanced Digital logic gate for a classic logic gate, the POP and AC analysis will give you the same results as before. However, with a digital control loop that is not stable due to discretization effects of the control signal, POP may not succeed because a Periodic Operating Point does not exist.